High performance *n*-channel organic field-effect transistors and ring oscillators based on C_{60} fullerene films

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We report on organic *n*-channel field-effect transistors and circuits based on C_{60} films grown by hot wall epitaxy. Electron mobility is found to be dependent strongly on the substrate temperature during film growth and on the type of the gate dielectric employed. Top-contact transistors employing LiF/Al electrodes and a polymer dielectric exhibit maximum electron mobility of 6 $cm^2/V\,s$. When the same films are employed in bottom-contact transistors, using SiO_2 as gate dielectric, mobility is reduced to 0.2 $cm^2/V\,s$. By integrating several transistors we are able to fabricate high performance unipolar (*n*-channel) ring oscillators with stage delay of 2.3 μs. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2387892]

To date hole transporting (*p*-type) organic small molecules and polymers are by far the most widely used materials for the fabrication of functional organic circuits based on unipolar logic architectures[1–9]. Electron transporting (*n*-type) organic semiconductors on the other hand have received considerably less attention[2,10] with very few circuit demonstrations.[11] This is mainly due to the poor operating stability of the vast majority of electron transporting organic field-effect transistors (OFETs) under ambient conditions with only few exemptions.[12–16] Among the relatively few known electron transporting molecules is the C_{60} fullerene with electron mobility, measured in oxygen and water free environment, on the order of 1 $cm^2/V\,s$.[17–19] Despite the high performance, however, C_{60} based transistors degrade rapidly upon exposure to ambient air.[11,18] In an effort to overcome this problem Horiuchi *et al.*[20] have reported on an efficient oxygen passivation method using a top coating of alumina layer sputtered under Ar atmosphere. As a result the stability of C_{60} transistors was considerably improved and showed no degradation upon exposure to air for a period of one month. This finding has renewed interest on fullerenes and use of C_{60} can now be envisioned not only in organic unipolar circuits but also in the much needed complementary architectures.[15,21,22] To this end a primary challenge is the further improvement of the operating characteristics of C_{60} OFETs and the demonstration of functional integrated circuits.

Here we report on high mobility electron transporting (*n*-channel) organic transistors and circuits based on C_{60} films grown by hot wall epitaxy (HWE).[17,23,24] Making use of this technique and in combination with suitable gate dielectrics, we are able to fabricate discrete electron transporting transistors and integrated ring oscillators with excellent performing characteristics.

Discrete top-contact transistors were fabricated on quartz glass substrates incorporating a predefined indium tin oxide (ITO) electrode acting as the gate terminal. Divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB), purchased from Dow Chemicals, was spin coated on the top of the quartz/ITO substrate as the gate dielectric. Following, a 300 nm thick film of C_{60} was grown by hot wall epitaxy[17] with the substrate maintained at different temperatures in the range of 100–250 °C. Finally, top-contact electrodes consisting of LiF/Al (0.6 and 60 nm, respectively) were evaporated under high vacuum (10^{-6} mbar) through a shadow mask. The channel length (L) and width (W) of the transistor were 30 μm and 1.5 mm, respectively. Bottom-contact field-effect transistors were made using heavily doped *n*-type Si wafers as the common gate electrode with a 200 nm thermally oxidized SiO_2 layer as the gate dielectric. Using conventional photolithography, gold source and drain electrodes were defined in a bottom-contact configuration with $L=10$ μm and $W=10$ mm. Due to the poor adhesion of evaporated gold on SiO_2, a thin (10 nm) interlayer of titanium (Ti) was employed between Au and SiO_2. The SiO_2 layer was treated with the primer hexamethyldisilazane (HMDS) prior to semiconductor deposition, in order to passivate its surface, followed by the growth of the C_{60} film by HWE. The detailed fabrication process of integrated circuits is described elsewhere.[6,11,16] Bottom-contact transistors and integrated circuits were annealed in vacuum (10^{-5} mbar) at 110 °C for 3 h prior to electrical characterization at room temperature.

To study the effects of substrate temperature (T_S) on the crystallinity of the C_{60}, films were characterized by means of atomic force microscopy (AFM) and x-ray diffraction (XRD) measurements. Figure 1(a) shows the AFM images for two 5 nm thick films of C_{60} grown at different T_S. It is evident

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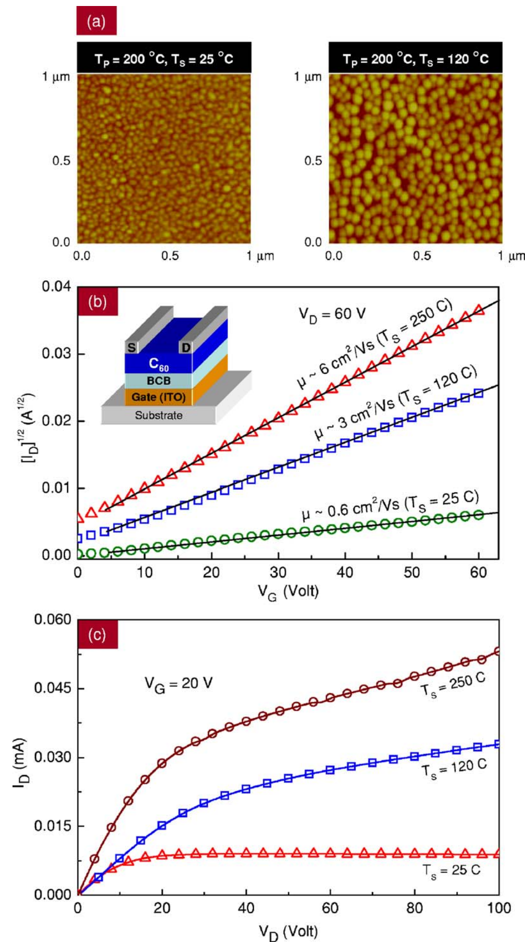

FIG. 1. (Color online) (a) AFM images of two 5 nm thick films of C_{60} grown by HWE on BCB at T_S=25 and 120 °C. T_P denotes the preheating temperature at which substrates were annealed prior to film deposition. (b) Square root of drain current ($I_D^{1/2}$) vs gate bias (V_G) obtained from three different transistors based on C_{60} films grown by HWE at different T_S. Inset shows the schematic structure of the top-contact transistors employed. (c) Output characteristics obtained from transistors based on C_{60} films grown at different substrate temperatures: T_S=25, 120, and 250 °C.

from this images that grain size increases with increasing T_S. In particular, for films grown at T_S=25 °C, the aerial density of crystallites is found to be in the order of ~500 crystallites/μm^2, whereas for films grown at 250 °C, this figure is reduced to ~370 crystallites/μm^2, indicating a larger grain size. Despite the morphological differences, however, both films exhibit the same highly crystalline structure, as determined by XRD measurements (data not shown), with the strongest 2θ-intensity diffraction peaks at 10.8°, 17.8°, and 20.9° 2θ, indexed as (111), (220), and (311), respectively. Our findings are in good agreement with previously published XRD data on thermally evaporated C_{60} films.[19,25]

To investigate the effects of grain size on the performance characteristics of C_{60} transistors, we fabricated top-contact devices [Fig. 1(b), inset] incorporating films grown at different substrate temperatures. Figure 1(b) shows the square root of the drain current ($I_D^{1/2}$) versus gate voltage (V_G) for three different devices at a drain voltage V_D=60 V. From this figure it is evident that in all devices $I_D^{1/2}$ depends linearly on V_G. From the linear fit in these plots, the saturated field-effect mobility was calculated employing the standard method[26] using a geometric capacitance value (as determined by capacitance-voltage measurements) of 1.2×10^{-9} F/cm^2.

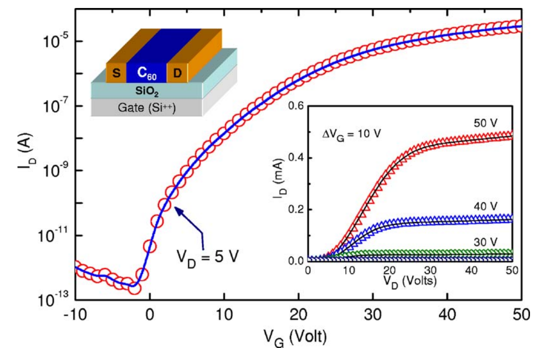

FIG. 2. (Color online) Room temperature transfer characteristic obtained from a bottom-contact C_{60} transistor (T_S=120 °C) employing SiO_2 as the gate dielectric. Inset diagram shows the device architecture employed. The inset figure displays the room temperature output characteristics of the transistor at different V_G.

It is evident that electron mobility increases from 0.6 cm^2/V s, for films grown at T_S=25 °C, to 3 cm^2/V s and 6 cm^2/Vs for films grown at T_S=120 and 250 °C, respectively. These results are in contrast with the findings of Kobayashi *et al.*[19] where the electron mobility showed no correlation with T_S. We note, however, that in the latter work measurements were performed on films grown on SiO_2 rather than polymeric dielectrics. An additional difference in our devices is the use of low work function (LiF/Al) source and drain electrodes that results to excellent electron injecting characteristics. Experimental evidences for the latter are provided by the linear dependence of I_D on V_D, at low voltages, shown in Fig. 1(c).

The operating characteristics of bottom-contact C_{60} transistors, using SiO_2 as the gate dielectric (Fig. 2, inset), were also investigated. Here C_{60} layers were grown by HWE at relatively low substrate temperatures (T_S=120 °C) in order to prevent decomposition of the HMDS layer used for SiO_2 passivation. Figure 2 shows a typical transfer characteristic obtained from a C_{60} transistor (L=10 μm, W=10 mm) measured at V_D=5 V. The inset figure shows the output characteristics at different V_G biases. The sigmoidal dependence of I_D on V_D at low drain voltages indicates the presence of a significant contact barrier. Despite that a high saturation mobility of 0.2 cm^2/Vs is calculated. We only report the mobility values in saturation simply because in this operating regime contact effects are known to reduce significantly.[11,27]

By integrating several bottom-contact transistors using the process flow chart for unipolar circuits,[6] we realized voltage inverters and ring oscillators. C_{60} films were grown by HWE at T_S=120 °C using polyvinylphenol as the gate dielectric. We employ relatively low T_S in order to avoid possible circuit damage caused by high temperature. Figure 3(a) shows the inverter circuitry and its symbolic representation. Owed to the switching characteristics of C_{60} OFETs the logic design employed here is the V_G=0 or "standard logic."[6] By integrating several inverters we are able to fabricate ring oscillators [Fig. 3(b), inset]. Our fastest circuits are fabricated employing a design rule of 2.5 μm with driver (W_D), load (W_L), and buffer (W_B) transistor widths of 300, 1200, and 5000 μm, respectively. Frequency measurements were performed by measuring the current flowing through a buffer transistor, whose gate was driven by the oscillator output, using a digital oscilloscope. The output signal of a seven-stage ring oscillator, operating at a supply voltage V_{DD}=80 V at room temperature, is shown in Fig. 3(b). Os-

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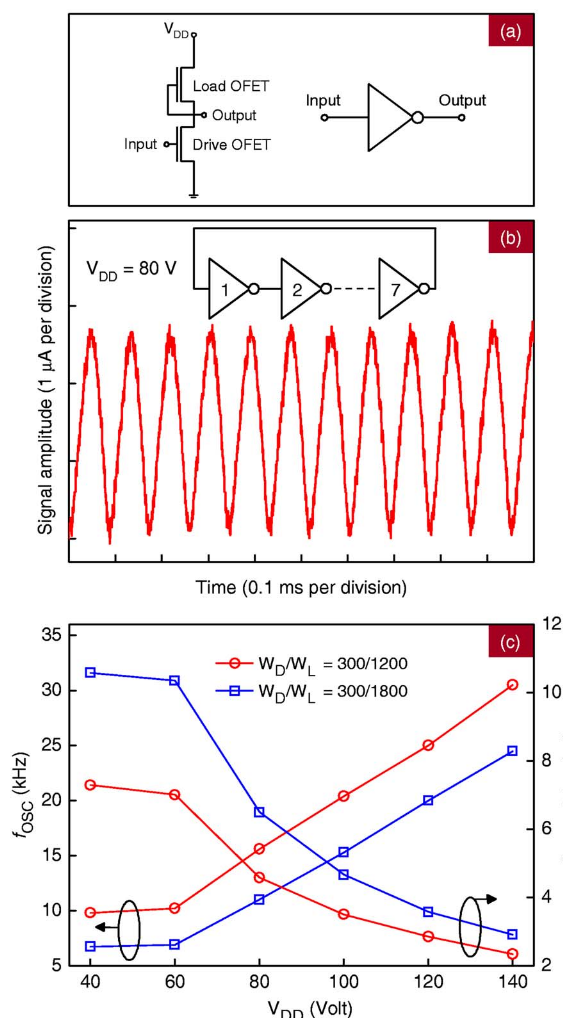

FIG. 3. (Color online) (a) Circuitry of the unipolar "standard logic" inverter used and its symbolic representation. (b) Output signal of the ring oscillator measured at V_{DD}=80 V in room temperature. Inset shows the schematic representation of the ring oscillator. (c) Oscillation frequency (f_{osc}) and calculated stage delay (τ) vs V_{DD} for two ring oscillators fabricated employing a design rule of 2.5. Red circles represent data obtained from a ring oscillator with a W_D/W_L=300/1200 while blue squares represent the signal from a ring oscillator incorporating larger load transistors with W_D/W_L =300/1800.

cillation frequency (f_{osc}) is found to depend strongly on V_{DD} as well as on the design rules employed. Figure 3(c) clearly demonstrates both effects. Here f_{osc} and calculated stage delay (τ),[16] for two different ring oscillators, are plotted versus V_{DD}. Red circles represent data obtained from a ring oscillator employing a design rule of L=2.5 μm with W_D/W_L =300/1200. For the second oscillator (blue squares) the same design rule applies but with W_D/W_L=300/1800. As can be seen the ring oscillator incorporating the small size load transistors (W_L=1200 μm) operates at a higher frequency ($f_{osc}\sim$30.5 kHz, $\tau\sim$2.34 μs) as compared with the ring oscillator employing load transistors with W_L=1800 μm ($f_{osc}\sim$24.5 kHz, $\tau\sim$2.9 μs). By increasing W_L to 3000 μm, the operating frequency is reduced further, clearly demonstrating the importance of design principles.

In summary, we have demonstrated top-contact n-channel organic transistors based on films of C_{60} grown by HWE with electron mobility of 6 cm^2/V s. A strong dependence of the electron mobility on the substrate temperature during film growth is observed. Increase of film grain size with increasing substrate temperature is believed to be the main reason for the improved electron mobility obtained. By using OFETs based on C_{60}, we were able to fabricate n-channel ring oscillators with a maximum operating frequency $f_{osc}\sim$30.4 kHz and a corresponding stage delay $\tau\sim$2.34 μs.

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